REMARKS

Claims 1, 4-6, 9 and 10 are rejected under 35 USC 103(a) as being unpatentable over Hill, Jr. (US 5,790,096), in view of Kubes et al. (US 6,035,180) and Takashimizu (JP 410091088 A) . Claims 2 and 7 are rejected under 35 USC 103(a) as being unpatentable over Hill, Jr. in view of Kubes et al. and Takashimizu, as applied to claims 1 or 6 above, and further in view of Shimoda (US 5,944,829). Claims 3 and 8 are rejected under 35 USC 103(a) as being unpatentable over Hill, Jr. in view of Kubes et al. and Takashimizu as applied to claims 1 or 6 above, and further in view of Nelson et al. (US 6,311,282 B1). Reconsideration and allowance of the claims is requested for the following reasons.

Applicant's invention as described in the specification and claimed in independent claims 1 and 6 is directed to a color organic electroluminescent display of the type having color emitting elements with different light emitting efficiencies, that saves power by determining the color of the elements having the highest efficiency; converting a color digital image to be displayed on the display to a monochrome image; and displaying the monochrome image using the determined color elements.

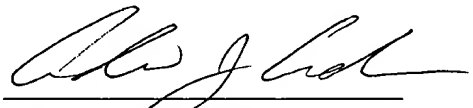
Hill Jr. discloses a controller for controlling all kinds of displays, including electroluminescent displays. As previously explained, in a first mode the controller uses only the green portion of a video signal to drive the red, green and blue inputs of a color display to produce a monochrome image. Thus, in this mode, all of the color elements are driven (see Col 7, lines 16-20) by the same amount, and no power saved thereby. In a second mode, the controller converts a color image signal to a monochrome signal according to the weighting chart in Table 1, and the monochrome signal is then used to drive a monochrome display having only one color of light emitting elements (see Col 7, lines 21-30). Thus, this mode also is not directed towards saving power on a color display. Neither of these modes suggest Applicant's invention, which is to save power by selectively driving only the color elements having the highest efficiency of a color display with the converted monochrome image signal.

The Examiner acknowledges that neither Hill nor Kubes specifically teach that the apparatus or methods thereof displays a converted monochrome image on a color display using only the most efficient color elements, and now attempts to further rely on Takashimizu for providing such teaching. Takashimuzu, however, does not appear to teach converting a color digital image to be displayed on the display to a monochrome image, and to selectively employ the most efficient color elements to save power when displaying the converted monochrome image. Rather, Takashimizu appears to teach an embodiment wherein when the display is used "in the case of displaying a screen of a monochrome" (i.e., when the incoming display signal is a monochrome signal to begin with), clocking signals to unused pixels/lines are turned off in order to save power otherwise expended on such clocking signals for unused pixels/lines. The Examiner's attention is directed, e.g., towards paragraphs [0070]-[0081] of the enclosed machine translation of Takashimizu, which has been obtained from the JPO internet website. Thus, while a means to save power when displaying a monochromatic screen is described, it is not taught to convert a color image to a monochrome to save power. Accordingly, the combination of Takashimizu with Hill and Kubes still fails to teach the present claimed invention.

Thus, even if the electroluminescent display of Kubes et al. were to be driven as the Examiner suggests by the controller of Hill Jr. in view of Takashimizu, in either the first or second modes of Hill of in the mode of Takashimizu, it would not result in Applicant's invention as disclosed and claimed since neither Hill Jr., Takashimizu nor Kubes et al. suggest driving only the highest efficiency color elements in a display when displaying a converted color image. It is believed therefore that the Examiner has still failed to state a *prima facie* argument for obviousness and Applicant is entitled to patentability of claims 1 and 6. The remainder of the claims depend from claim 1 or 6 and are believed to be patentable for at least the same reasons. It is believed that the claims in the application are allowable over the prior art and such allowance is respectfully requested.

In view of the foregoing remarks, reconsideration of this patent application is respectfully requested. A prompt and favorable action by the Examiner is earnestly solicited. Should the Examiner believe any remaining issues may be resolved via a telephone interview, the Examiner is encouraged to contact Applicants' representative at the number below to discuss such issues.

Respectfully submitted,



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[Claim(s)]
[Claim 1] a luminescence cel which constitutes one pixel in matrix display equipment which arranges two or more pixels in the shape of a matrix, and changes -- four -- carrying out -- this -- matrix display equipment which two of four luminescence cels are the luminescence cel of the same color, and is characterized by making a luminescence cel of this same color smaller than a luminescence cel of other colors.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the matrix display equipment of a configuration of having been suitable for enabling reduction of the reactive power accompanying carrying out the charge and discharge of the drive electrode stray capacity on the occasion of the drive of the panel of this equipment in more detail about the matrix display equipment like a plasma display panel (it calling for short Following PDP).
[0002]
[Description of the Prior Art] A matrix display panel is a display panel which consists of two or more drive electrodes linked to the display device and each display device as a pixel arranged in the shape of a matrix, and an image is displayed by changing each luminescence brightness or permeability of a pixel (display device) with the driving signal impressed to each drive electrode.
[0003] As a scan method of such a panel, they are "display device and the equipment latest technology, for example. Generally the method of impressing a pulse to electrodes other than the scan electrode which impresses a picture signal to the timing always defined irrespective of the contents of an image is learned as indicated by '85"(comprehensive technical publication) 188 page -190 page. Furthermore, when image data is not inputted into JP,61-200593,A like a publication but all the line electrodes change into the condition of not choosing, the drive method of reducing the power consumption which does not contribute to a display by lowering the frequency of the pulse impressed to each matrix electrode is learned.
[0004]
[Problem(s) to be Solved by the Invention] Although the charge and discharge of this stray capacity are performed by stray capacity's accompanying the drive electrode of a matrix display panel, and impressing a pulse to a drive electrode, the power loss accompanying this charge and discharge is reactive power which does not contribute to a display. Especially, like EL (electroluminescence panel) or PDP, when an impression

pulse voltage is high, this reactive power becomes large.
[0005] As shown in above-mentioned JP,61-200593,A as this cure, when the image which all the line electrodes of a display panel should be un-choosing, and should be displayed does not exist, there is a method of reducing loss by lowering an impression pulse frequency. However, the method shown in this JP,61-200593,A was a method which cannot reduce power loss when only some line electrodes change into the condition of not choosing, and lowers the frequency of an impression pulse, and since it did not necessarily abolish an impression pulse, it had the problem that reactive power could not be lost completely.
[0006] By stopping impression of the driving pulse to an applicable line, when the purpose of this invention detects the input data for every line of the matrix which consists of a row and column and an applicable line is un-choosing It is in offering the matrix display equipment which has the array of the matrix luminescence cel which has much more effect in reduction of this reactive power with the matrix display equipment which reduces reactive power also when only a part changes into the condition of not choosing, among all line electrodes.
[0007]
[Means for Solving the Problem] a luminescence cel which constitutes one pixel in matrix display equipment which the above-mentioned purpose arranges two or more pixels in the shape of a matrix, and changes -- four -- carrying out -- this -- two of four luminescence cels are the luminescence cel of the same color, and it is attained by making a luminescence cel of this same color smaller than a luminescence cel of other colors.
[0008]
[Function] In the drive of the panel of matrix display equipment, the driving pulse output actuation to a line electrode is controlled for every line electrode based on the contents for every horizontal scan period of an input picture signal. By this, even when only some line electrodes of a matrix display panel are un-choosing, a driving pulse is not impressed to an applicable line electrode, but loss by the reactive power consumed in connection with the stray capacity charge and discharge of a line electrode can be reduced.
[0009] the luminescence cel which constitutes one pixel in matrix display equipment in that case -- four -- carrying out -- this -- if it is made for two of four luminescence cels to be the luminescence cel of the same color, each luminescence cel of the two same colors is connected to the same drive electrode. Then, what is necessary is just to make only the luminescence cel of G emit light, when displaying, monochromatic screen, for example, green screen. The line in which the pixel of G does not exist does not need to drive. That is, by controlling actuation of an electrode drive according to a display condition, when always impressing a driving pulse, the power consumption which this electrode drive takes can be reduced to one half. Moreover, the luminescence brightness of each color can be made into homogeneity by making magnitude of the two same luminescence cels smaller than the magnitude of the luminescence cel of other colors.
[0010]
[Example] The principle of operation of the matrix display equipment by this invention is explained using a drawing below. Drawing 2 is the block diagram, i.e., the block diagram showing the principle of operation for the memory mold plasma display panel (PDP) drive circuit which has an auxiliary anode, showing the principle of operation of the

matrix display equipment by this invention.
[0011] The configuration shown in this drawing consists of the signal input terminal 1, the synchronousr-control circuit 2, A/D conversion and a memory circuit 3, the auxiliary anode pulse generating circuit 4, the anode plate pulse generating circuit 5, the cathode pulse generating circuit 6, the auxiliary anode driver 7, the cathode driver 8, the switch train 9, a memory type PDP10, and a power recovery circuit 100.
[0012] The discharge cels P11-Pnm which have an anode plate A, Cathode K, and an auxiliary anode SA a memory type PDP10 in a longitudinal direction (horizontal) m pieces, each discharge cel which has the structure arranged in n lengthwise directions (perpendicular direction), and is located in a line with a longitudinal direction for every single tier P11-P1m, P21-P2m, and Pn1-Pnm It An(s). every -- n anode plate drive electrodes A1 which come to pull out an anode plate A in common, A2, and .... And n cathode drive electrodes K1 which come to pull out Cathode K in common, and K2, ..., Kn, and each discharge cels P11-Pn1 for every party on a par with a lengthwise direction, P12-Pn2, ..., the auxiliary anode drive electrode S1 that comes to pull out an auxiliary anode SA in common for every Pm-Pnm, and S2, .., Sm from -- it changes.
[0013] these drive electrode A1 -An, K1 -Kn, and S1 - Sm **** -- the anode plate stray capacity CA1-CAn, the cathode stray capacity CK1-CKn, and the auxiliary anode stray capacity CS1-CSm accompany, respectively. Moreover, the power recovery circuit 100 consists of a switch 11-1 - 11-n, 12-1 - 12-n and 14-1 - 14-n, an inductor 13-1 - 13-n, a capacitor 15, and a power supply terminal 200. It sets in the configuration of drawing 2 and is anode plate drive electrode A1 -An of a memory type PDP10. The example which applied the power recovery circuit is shown.
[0014] Hereafter, circuit actuation of drawing 2 is explained. A video signal (video signal) is inputted into the signal input terminal 1. Based on this input signal, a synchronizing signal required for actuation of each circuit is formed in the synchronousr-control circuit 2. A/D conversion and a memory circuit 3 change and carry out memory of the input signal to a digital signal. Based on the input video signal by which memory was carried out, a signal (auxiliary anode pulse) required for an auxiliary anode drive is formed in the auxiliary anode pulse generating circuit 4. This auxiliary anode pulse minds the auxiliary anode driver 7, and is the auxiliary anode drive electrode S1 - Sm. It is impressed.
[0015] The cathode pulse generating circuit 6 forms a signal (cathode pulse) required for a cathode drive based on the signal from the synchronousr-control circuit 2. This cathode pulse minds the cathode driver 8, and is cathode drive electrode K1 -Kn. It is impressed.
[0016] The anode plate pulse generating circuit 5 forms a signal (anode plate pulse) required for an anode plate drive based on the signal from the synchronousr-control circuit 2. Closing motion of the switch 11-1 which constitutes the power recovery circuit 100 based on the information on this anode plate pulse and the information on an auxiliary anode pulse - 11-n, and a switch 9-1 - 9-n is controlled, and it is anode plate drive electrode A1 -An. A driving pulse (said anode plate pulse and equivalent timing) is impressed.
[0017] As mentioned above, three kinds of pulses, an auxiliary anode pulse, a cathode pulse, and an anode plate pulse, are needed for driving the memory type PDP10 in the configuration of drawing 2 . The timing relationship of these pulses is explained using the example of a wave of operation of drawing 3 .

[0018] Cathode pulse Kp It is for carrying out the vertical scanning of the memory type PDP10. Cathode drive electrode K1 Pulse k0 By impressing, the vertical scanning (subfield scan) of 1 cycle is performed. Furthermore, at drawing 3 , it is a pulse k1, k2, and k3. Performing the vertical scanning (subfield scan) to depend is shown. It carries out for carrying out such, and the screen for the 1 field in the usual television is constituted by two or more subfield screens twisted to the vertical scanning of multiple times. In addition, although auxiliary discharge occurs by impressing a cathode pulse between the cathode-auxiliary anodes (K-SA) of the discharge cels P11-Pnm, since this auxiliary discharge is feeble, it cannot carry out view ** from the outside of a memory type PDP10.

[0019] Auxiliary anode pulse Sp It is for carrying out the horizontal scanning of the memory type PDP10, and is said cathode pulse Kp. It is impressed according to timing. For example, it is 8 bits about an input video signal. Memory of the information which carried out A/D conversion shall be carried out to A/D conversion and a memory circuit 3. Said cathode pulse Kp Inside and pulse k0 Auxiliary anode pulse Sp based on the lower bit information on the digital data by which A/D conversion was carried out to compensate for the vertical scanning to depend The auxiliary anode drive electrode S1 - Sm It impresses. Thus, the 1st subfield screen based on the lower bit information on a video signal is displayed.

[0020] It is the cathode pulse k1, k2, ...k7 similarly. Auxiliary anode pulse Sp based on [one by one] the next high-order-bit information on a video signal to compensate for each vertical scanning to depend It impresses. Thus, a sequential indication of the subfield screen of eight sheets based on the information for every bit is given.

[0021] In addition, auxiliary anode pulse Sp Although the main stroke transferred from the above-mentioned auxiliary discharge by impressing between the cathode-anode plates of the discharge cels P11-Pnm (between K-A) occurs, since this main stroke is feeble, the display screen in this phase does not look almost.

[0022] Anode plate pulse Ap It is for maintaining the main stroke between K-A produced by transition of said auxiliary discharge, and the luminescence brightness of a discharge cel can be decided by the impression number of this pulse. namely, cathode pulse k0 the 1st vertical scanning to depend -- doubling -- anode terminal A1 -An a0 every -- an anode plate pulse is impressed.

[0023] Thus, the discharge cel chosen at the time of the 1st vertical scanning is a0. Luminescence of a time is repeated. It doubles with the 2nd and 3rd .... and the 8th vertical scanning similarly, and is a1, and a2, .., a7, respectively. Luminescence of a time is repeated. For example, if a0 =4, a1 =8, a2 =16, ..., a7 =512, a discharge cel can perform the screen display of a repeat and 256 gradation for luminescence of a total of 0, 4 and 8, or ..1020 time by total of eight subfield displays.

[0024] In addition, anode plate pulse Ap Since the main stroke between K-A produced by impressing is stronger than the main stroke between K-A by transition of the above-mentioned auxiliary discharge, it depends for most luminescence brightness of a discharge cel on an impression anode plate pulse number.

[0025] the control pulse q0 of the change impressed to a switch 9-1, and q1 q2 .... anode plate drive electrode A1 the timing which controls impression of an anode plate pulse and a switch 9-1 closes -- doubling -- the output pulse from the power recovery circuit 100 -- every [a0, a1, and / a2 ..] -- anode plate drive electrode A1 It is impressed. The pulse

which was late for the pulse impressed to a pre- switch 1H (1 level period) every is impressed to a switch 9-2, 9-3, and .... Thus, a switch 9-1 - 9-n are minded, and it is anode plate drive electrode A1 -An. The pulse impressed is the above-mentioned anode plate pulse a0 -a7. It completely becomes the same.

[0026] Next, it explains using the wave form chart of operation showing actuation of the power recovery circuit 100 in drawing 2 in the principle circuit and drawing 5 which are shown in drawing 4 . The switch 9 shows the case where it closes, with the circuit diagram which drawing 4 took out 1 set of unit circuits in the power recovery circuit 100 of drawing 2 , and was shown. That is, this circuit mainly consists of switches 11, 12, and 14, an inductor 13, a capacitor 15, and a power supply terminal 200. Moreover, resistance 201-1 and a capacitor 201-2 show effective resistance, such as a switch in an actual circuit, and an inductor, and stray capacity collectively. A capacitor 202 is equivalent to the anode plate stray capacity CA.

[0027] In the initial state of the time of day t= 0 shown in drawing 5 , switches 11 and 14 are OFF, and a switch 12 is ON, and it is the voltage Vc of a power supply terminal 200. Receiving, the terminal voltage of a capacitor 15 is Vc/2. Since a switch 12 is ON, a capacitor 202 is in discharge exit status. Therefore, the terminal voltage Vo It is 0. Moreover, the capacity of a capacitor 15 is large enough and the terminal voltage presupposes that it is still Vc/2 in the following actuation.

[0028] Time of day t1 A switch 12 is turned OFF and a switch 14 is turned ON. Current IL according to resonance to a capacitor 202 side through this moment and a capacitor 15 to the inductor 13 It flows. If the value of Co and resistance 201-1 is set [the value of an inductor 13 / the value of L and a capacitor 201-2] to R for the value of Cf and a capacitor 202, they are terminal voltage Vo and the resonance current IL as what has the small value of R. It is expressed as follows.

[0029]

V0= (Vc/2) -- [-- 1 1 {(a/omega) sinomegat+cosomegat} and exp(-at)] .... (1)

IL =(Vc/R) and (a/omega) sinomegat-exp (-at) .... (2)

[0030] It is here. a=R/2L omega= {(1-/LC) -a2} 1/2 C=Cf+C0 However (1-/LC), > a2 .... (3)

Come out and it is (oscillating resonance conditions of an LCR circuit).

[0031] Above From (1) type, it is terminal voltage Vo. As shown in the condition [A] of drawing 5 , it is maximum Vo=(Vc/2) {1+exp(-a pi/omega)} =Vc in time-of-day t2=pi / 2omega at Vo=(Vc/2) {1- (a/omega) and exp (- api / 2omega)} **Vc / 2 time-of-day t3= pi/omega. It reaches.

[0032] on the other hand, the resonance current IL Terminal voltage Vo the wave which progressed only pi/2omega -- [F] -- becoming -- time of day t1 and t3 -- IL =0 and time of day t2 -- coming out -- maximum IL =IA = (Vc/2) and (a/omega), and exp (- api / 2omega) It becomes.

[0033] At time of day t3, a switch 14 is turned OFF and a switch 11 is turned ON. In time of day t3, the terminal voltage Vo of a capacitor 103 has reached supply voltage Vc mostly, and is fixed to the voltage Vc of a power supply terminal 200 by turning on a switch 11.

[0034] Thus, the standup of the pulse shown in drawing 5 is formed. Time amount tr of this pulse required for starting 0 to 100% tr = pi/omega 1-/(LC)-R2 / [=pi// {/ / / (4L2) /}] 1 / 2 **pi (LC) 1/2 .... (4)

It is expressed.
[0035] However, time of day t3 Terminal voltage Vo of the moment of turning ON a switch 11 It is completely supply voltage Vc. It is not in agreement. therefore, the moment that a switch 11 is turned on -- a capacitor 202 -- supply voltage Vc up to -- it will charge.
[0036] Since this charge is performed through resistance 201-1 from a power supply terminal 200 side, the standup by the transient phenomenon of CR is added correctly. The round mark in drawing 5 [D] showed this (a round mark [E] is the same). However, with this configuration, the portion of a round mark [D] is not included in the time amount required for starting as what has the sufficiently small value of resistance. It is time amount tr =1microsecond actually required for being 100pF and about 50ohms even if the value of C and R is large, setting CR time constant at this time to CR=5ns, and starting. It can ignore enough to the pulse of a degree.
[0037] After predetermined time amount progress and time of day t4 A switch 11 is turned OFF and a switch 14 is turned ON. this time -- the terminal voltage of a capacitor 15 -- the terminal voltage of Vc/2 and a capacitor 202 -- Vc it is -- since -- the current of an LCR resonance circuit flows from a capacitor 202 side to a capacitor 15 side at the moment of turning ON a switch 14.
[0038] Hereafter, it is voltage Vo at the same circumstances as the standup [A] of the pulse in drawing 5 . It changes, as shown in a condition [C]. Current IL in this process It flows to the time of a pulse standup, and hard flow, and becomes like a condition [G]. Time of day t6 Terminal voltage Vo A switch 12 is turned ON at the moment of becoming min.
[0039] Thus, the circuit of drawing 4 ends 1 cycle and return and one pulse are formed in an initial state. Time amount tf which falling of this pulse takes Time amount tr which the above-mentioned standup takes It is completely the same and is tf **pi(LC) 1/2. It becomes.
[0040] ****** P lost while performing actuation whose circuit of drawing 4 is 1 cycle is ** time-of-day t1 -t3. Current IL which flows resistance 201-1 in the condition [A] at the time of LCR resonance Loss P1 ** time of day t3 to depend Loss P2 by the transient current which flows to resistance 201-1 in the transition stage [D] of CR produced by turning ON a switch 11 [0041] ** Current IL which flows resistance 201-1 in the condition [C] at the time of LCR resonance of time of day t4-t6 Loss P3 ** time of day t6 to depend It is the sum total of the loss P4 by the transient current which flows to resistance 201-1 in CR transition stage [E] produced by turning on a switch 12. It is [0042] when it asks for this by count.
[Number I]

[0043] Furthermore, the above If (3) and (4) types are used P** (tr/4) and (R/L) CVc2 .... (5)

It becomes.
[0044] Above From (5) types, only the part which hung a coefficient (tr/4) and (R/L) compared with the method of loss of the circuit of drawing 4 switching supply voltage with a switch, and impressing a pulse becomes small. For example, when tr =1microsec, R= 50 ohms, and C= 100pF, the required inductance L is L**(tr/pi)2/C**1mH. At this time, it is -(tr/4) (R/L)**0.0125, and loss of the circuit of drawing 4 can be managed with 0.0125xCVc2 per one pulse, and it turns out that it is small compared with CVc2.
[0045] Although an anode plate pulse is formed as mentioned above, this actuation is controlled by the signal impressed by the anode plate pulse generating circuit 5. The example of a configuration of the anode plate pulse generating circuit 5 is shown in drawing 6 . Drawing 6 consists of a signal input terminal 5-1 which inputs the signal from the delay element (Delay) 52-1 of 51 or n ROMs, 52-2, ..., the delay circuit 52 that consists of 52-n, and the synchronousr-control circuit 2, an output terminal 5-2 which outputs an anode plate pulse, and a signal input terminal 5-3 which inputs the signal from an auxiliary anode pulse.
[0046] Into ROM51, memory of the wave of an anode plate pulse is carried out, and it is read based on the synchronousr-control signal inputted from an input terminal 5-1. It is a read-out signal from ROM51 B1 They are B-2, ..., Bn about the signal which reaches, and considers as B1', and sequential delay is carried out in a delay circuit 52, and is acquired. And it considers as B-2', .., Bn'. However, since the signal of Bn' does not have the delay circuit of the next step which should be transmitted, it is not necessary to output. Therefore, it omitted in drawing 6 .
[0047] These B1 -Bn It reaches and the signal of B1' - Bn' is anode plate drive electrode A1 -An, respectively. It is the same timing as the signal impressed, and becomes the power recovery circuit 100 shown in drawing 2 , and the control signal of a switch 9 via an output terminal 5-2. In addition, B1 -Bn B1' - Bn' is the same signal mutually.
[0048] In order for each cel of a memory type PDP10 to emit light as mentioned above, it is required to impress three kinds of pulses, a cathode pulse, an anode plate pulse, and an auxiliary anode pulse. Among these, an auxiliary anode pulse is formed based on the signal which changed the input video signal into digital quantity by A/D conversion and memory 3, and the horizontal scanning of a memory type PDP10 is performed by this.
[0049] On the other hand, what is necessary is to carry out memory of the wave to ROM51, and just to read these based on a synchronousr-control signal, since what is necessary is just to output a cathode pulse and an anode plate pulse to the always defined timing. Therefore, it will be determined by whether an auxiliary anode pulse is impressed whether each cel of a memory type PDP10 emits light.
[0050] By this, when all the P11-P1m cels of one line do not emit light, the auxiliary anode pulse will be impressed. However, since an anode plate pulse is impressed to the timing always defined with respect to the contents of an image that there is nothing as mentioned above, even when all the cels of one line do not emit light, an anode plate pulse is the anode plate drive electrode A1. It will be impressed, the charge and discharge of stray capacity CA 1 will be performed, and loss is produced by this.
[0051] For this reason, it sets in the circuit of drawing 2 and they are the auxiliary anode drive electrode S1 - Sm. When a pulse is not outputted to all, the control signal for a drive halt of an anode plate pulse generating circuit is outputted. A configuration as shown in drawing 7 as this method can be considered.

[0052] They are the circuit 41 in which drawing 7 is the circuit diagram showing the example of the auxiliary anode pulse generating circuit 4 in drawing 2 , and this circuit forms an auxiliary anode pulse based on the signal input terminal 4-1 which inputs the signal from A/D conversion and memory 3, and an input signal, the auxiliary anode pulse S1 - Sn. It consists of terminals 4-3 which output the output signal of the output terminal 4-2 to output, NOR circuit 42, and a NOR circuit.
[0053] In NOR circuit 42, they are the auxiliary anode pulse S1 - Sm. It is inputted. As mentioned above, since the luminescence brightness of each cel of a memory type PDP10 is decided by the number of the anode plate pulse impressed and an auxiliary anode pulse only decides whether a cel emits light, the value of an auxiliary anode pulse is good binary [of 0 and 1].
[0054] Therefore, S1 - Sm when all the cels of one line do not emit light Only when it is 0 altogether, the output of NOR circuit 42 is outputted from an output terminal 4-3. This output is impressed to the input terminal 5-3 in drawing 6 . Since it is not necessary to impress an anode plate pulse when all a party's cels of all do not emit light, actuation of ROM51 and a delay circuit 52 is controlled, and it is made not to output a pulse based on the signal from the signal input terminal 5-3.
[0055] In addition, ROM51 and a delay circuit 52 are B1, although B1, B-2, and .... and two signals which are B1', B-2', and .. are outputted as shown in drawing 6 . B1', B-2 and B-2', and .. are the same signals mutually. Thereby, ROM51 and a delay circuit 52 are signal B1 -Bn to an output terminal 5-2, transmitting signal B1', B-2', and .... to the delay circuit of the next step respectively. An output is controllable according to an individual.
[0056] Thus, when all the cels of one line do not emit light, it is made not to generate an anode plate pulse, and it is anode plate drive electrode A1 -An. He is trying for loss by the charge and discharge of the accompanying stray capacity CA1-CAn not to arise.
[0057] Furthermore, in drawing 2 , since eight subfield scans constitute the image of the 1 field, if total, even when [which is the 1 field] the image is being displayed, there may be no necessity of scanning in a subfield scan (an anode plate drive electrode being driven), and, thereby, loss can be reduced further.
[0058] Drawing 8 is the example which constituted the power recovery circuit 100 of drawing 2 using the variable inductor 13. drawing 2 -- setting -- anode plate drive electrode A1 -An every -- although the power recovery circuit was prepared -- the circuit of drawing 8 -- one power recovery circuit 100 -- two or more anode plate drive electrodes A1-An It has the composition of impressing an anode plate pulse. each anode plate drive electrodes A1-An **** -- since stray capacity CA1-CAn accompanies, the resonance capacity of a power recovery circuit changes with the switching conditions of a switch 9.
[0059] Each stray capacity CA1-CAn is the almost same value, and sets this with CA0. Therefore, supposing eight of n switches 9 are turned on, the resonance capacity C of the power recovery circuit 100 will serve as C=8CA0.
[0060] Time amount tr which the standup of a pulse will take if the resonance capacity C of the power recovery circuit 100 changes Above-mentioned It changes according to (4) types. This is avoided and it is tr. In order to keep it the same, a variable inductor 13 is used and the power recovery circuit 100 consists of configurations of drawing 8 .
[0061] The example of a configuration of a variable inductor 13 is shown in drawing 10 . Drawing 10 is a circuit which compounds j inductors 21-1 which switched j switches 31

and were connected to each switch - 21-j by parallel connection. The terminal 13-1 in drawing 10 , 13-2, and 13-3 are the terminals linked to the switch 14, the switches 11 and 12, and the anode plate pulse generating circuit 5 in drawing 8 , respectively.
[0062] an inductor 21-1L0 and 21-2 -- L0/2, and -- the value LL0 of an inductance compoundable [with closing motion of a switch 31] if 21-j is set to L(1/2j-1) 0, L0/2, --, L -- it is 0/(2j-1)0. Since the resonance capacity C changes with 0, CA0, 2CA0, --8CA0, --nCA0 2j-1 >=n .... (6)
Using the inductance of j integers of ******** min, adjustable [of the inductor wardrobe L] can be carried out to the value of C of arbitration, and it is CL=CA 0L0 (fixed).
It can become.
[0063] For example, when n= 480, it is good to use nine inductors. Closing motion of a switch 31 is performed based on the signal from the cathode pulse generating circuit 5 like the after-mentioned. In addition, for the output pulse of the power recovery circuit 100 of drawing 8 , as shown in drawing 9 , repeat frequency and pulse width are the anode plate pulse Ap. It is the same, for example, is the continuous pulse. this -- closing motion of a switch 9 -- every [a0, a1, a2, and / ....] -- anode plate drive electrode Ap It is impressed.
[0064] The example of a configuration of the anode plate pulse generating circuit 5 for controlling the variable inductor 13 of drawing 10 to drawing 11 is shown. Drawing 11 adds an encoder 53 to the circuit of drawing 6 . B1 -Bn in the number of the switch closed with a switch 9 at the power recovery circuit 100 side to control closing motion of the switch 31 in the variable inductor circuit of drawing 10 , i.e., drawing 11 , What is necessary is just to use the data which binary-ized the pulse number. At drawing 11 , it is B1 -Bn. Decimal -> code conversion is carried out with the encoder 53 of a binary, it outputs from a terminal 5-4, and closing motion of a switch 31 is controlled by this.
[0065] In addition, various configurations as a configuration of the delay circuit shown in drawing 6 and drawing 11 can be considered. As the example, the example of a configuration of a delay circuit is shown in drawing 12 . 502 is Pulse Bi by being a NAND circuit and impressing a control pulse from a terminal 5-3. An output can be suspended.
[0066] It is anode plate drive electrode A1 -An in the power recovery circuit 101 which becomes drawing 13 from two lines. The configuration to drive is shown. They are the anode plate drive electrodes A1-aluminum divided into 2 sets using the power recovery circuit 101 which is only the difference which transposes the power recovery circuit 100 in drawing 8 to the power recovery circuit 101, and consists of two lines fundamentally, and aluminum+1-An. It drives. A variable inductor 13-1 and 13-2 are the anode plate drive electrode A1 divided into 2 sets - aluminum, respectively. aluminum+1-An It is controlled based on the information on the anode plate pulse to impress. In addition, a capacitor 15 can be made common although the power recovery circuit 101 consists of two lines.
[0067] They are the case where the total value of the anode plate stray capacity CA1-CAn is too large to drive only in one power recovery circuit although the configuration of having been shown in drawing 8 as a configuration is easier, and anode plate drive electrode A1 -An. There are too many numbers, and when neither the adjustable width of face of a variable inductor 13 nor control fulfills demand, the configuration which divides a power recovery circuit into two lines is also effective. Furthermore, the method of

dividing a power recovery circuit into two or more lines, and driving it is also considered.
[0068] Drawing 14 is an example of a configuration which does not apply a power recovery circuit which has so far been described. Although loss becomes large with the configuration of drawing 14 compared with the case where a power recovery circuit is applied, it is not necessary to use an inductor. Although a circuit scale will become large if a power recovery circuit is used since an inductor cannot be used for an integrated circuit, with the configuration of drawing 14 , it is not necessary to use an inductor for example, all circuits can be IC-ized, and a scale can be made small.
[0069] Moreover, in drawing 14 , it is considering as the configuration which also controls actuation of the cathode pulse generating circuit 6 with the anode plate pulse generating circuit 5, and when generating a pulse by the always defined pattern, loss can be reduced according to a display condition. In addition, although the case where actuation of the anode plate pulse generating circuit 5 or the cathode pulse generating circuit 6 was controlled by the configuration of drawing 2 - drawing 14 was shown, the same effect can be acquired even when controlling a switch 9 and actuation of the cathode driver 8.
[0070] Drawing 15 is drawing showing the pixel arrangement of a memory type PDP10 which is consulted when you understand the example (after-mentioned) of this invention. Each pixel of R, G, and B of the memory type PDP10 of drawing 15 is the so-called thing of the arranged horizontal stripe pixel arrangement a horizontal single tier every, respectively.
[0071] In addition, in drawing 15 , the anode plate drive electrode and the cathode drive electrode are omitted. In drawing 15 , when displaying a monochromatic screen, for example, a red screen, only the pixel of R emits light and the pixel of G and B does not emit light. Therefore, it is not necessary to impress an anode plate pulse and a cathode pulse to the line by which the pixel of G and B has been arranged. That is, according to a display condition, actuation of an anode plate drive circuit and a cathode drive circuit can be controlled, and power consumed compared with the case where a pulse is always impressed, for an anode plate and a cathode drive by making it not impress a pulse can be set to one third.
[0072] Drawing 1 is drawing shown as one example of this invention which applied the principle of operation which already described the memory type PDP10 which has arranged each pixel of R, G, and B so that drawing 15 may differ. In drawing 1 , the memory type PDP10 is constituted so that each pixel may accomplish 1 set by four, R, G, G, and B. By things, as pixel arrangement of a memory type PDP10 is shown in drawing 1 making it be the above, all the lines of a memory type PDP10 can contain only two kinds of pixels among three kinds of pixels, R, G, and B, respectively.
[0073] Moreover, in drawing 1 , each of two pixels of G in 1 set of R, G, G, and B of pixels is connected to the same drive electrode (3, an auxiliary anode drive electrode, an anode plate drive electrode, and a cathode drive electrode). Therefore, although it divided into two lines in 1 set of pixels and being arranged, when driving this, two pixels of G can be treated like the case where it is in the same line.
[0074] What is necessary is just to make only the pixel of R emit light in drawing 1 , when displaying a monochromatic screen, for example, a red screen. Since the pixel of R is arranged every other line in drawing 1 , the line in which the pixel of R does not exist does not need to drive. That is, by controlling actuation of an anode plate and a cathode

drive circuit according to a display condition, when always impressing a driving pulse, the power consumption of this drive circuit can be reduced to one half.
[0075] In addition, although only two pixels of G are contained in 1 set of pixels in drawing 1 , he is trying for the luminescence brightness of R, G, and B each pixel to become homogeneity by making magnitude of the pixel of G smaller than the pixel of R and G. Moreover, although considered as the configuration in which two pixels of G are contained in 1 set of pixels in drawing 1 , the same effect is acquired even if it transposes this to the pixel of R or B.
[0076] Furthermore, although the case where detected the output pulse of the auxiliary anode pulse generating circuit 4 in drawing 2 - drawing 14 , and the driving pulse impression to a line electrode was controlled was shown, the same effect can be acquired even when detecting the output of A/D conversion and a memory circuit 3, i.e., the impression digital signal to the auxiliary anode pulse generating circuit 4.
[0077] Drawing 16 is an example of a configuration in the case of performing the usual field scanning which impresses a driving pulse to the 1 field by a unit of 1 time at each anode plate drive electrode instead of a subfield scan which has so far been described.
[0078] In drawing 16 , the detector 60 which detects the voltage level of an input video signal is formed, when it is detected that the voltage level of 1 horizontal scanning period in which an input video signal has this detector 60 is below fixed level, actuation of the anode plate pulse generating circuit 5 is controlled with the output of this detector 60, and he is trying not to impress a driving pulse to the anode plate drive electrode to which the pixel in which the signal of said horizontal scanning period should be written was connected. Thereby, the power loss by unnecessary driving pulse impression can be reduced.
[0079] In addition, although actuation of the anode plate pulse generating circuit 5 is controlled by drawing 16 by detecting the voltage level of an input video signal, it is clear that the same effect is acquired also by the method shown by drawing 2 - drawing 14 which control an anode plate pulse generating circuit by the input digital signal to the auxiliary anode pulse generating circuit 4 or existence of this auxiliary anode pulse.
[0080]
[Effect of the Invention] Since impression of a driving pulse is controllable for every line drive electrode based on the contents of the input picture signal according to this invention Although loss by the reactive power which can be prevented from impressing a driving pulse and is consumed by the stray capacity charge and discharge of a line drive electrode can be reduced when an applicable line drive electrode is un-choosing the luminescence cel which constitutes one pixel in matrix display equipment in that case -- four -- carrying out -- this -- if it is made for two of four luminescence cels to be the luminescence cel of the same color, each luminescence cel of the two same colors is connected to the same drive electrode.
[0081] Then, what is necessary is just to make only the luminescence cel of G emit light, when displaying, monochromatic screen, for example, green screen. The line in which the pixel of G does not exist does not need to drive. That is, by controlling actuation of an electrode drive according to a display condition, when always impressing a driving pulse, there is an advantage that the power consumption which this electrode drive takes can be reduced to one half. Moreover, when two make the luminescence cel of the same color smaller than other luminescence cels, it is effective in the luminescence brightness of

each color being made to homogeneity.

[Brief Description of the Drawings]
[Drawing 1] It is drawing showing pixel arrangement of one example of this invention.
[Drawing 2] It is the block diagram showing the principle of operation of the matrix display equipment by this invention.
[Drawing 3] It is the timing chart of the main driving pulses used in circuit actuation of drawing 2 .
[Drawing 4] It is a circuit diagram for explaining details actuation of the power recovery circuit in drawing 2 .
[Drawing 5] They are the voltage of the important section in the circuit of drawing 4 , and a current wave form Fig.
[Drawing 6] It is the circuit diagram showing the example of the anode plate pulse generating circuit in drawing 2 .
[Drawing 7] It is the circuit diagram showing the example of the auxiliary anode pulse generating circuit in drawing 2 .
[Drawing 8] It is the block diagram showing another example of the principle of operation.
[Drawing 9] It is the timing chart of the main driving pulses used in circuit actuation of drawing 8 .
[Drawing 10] It is the circuit diagram showing the example of a configuration of the variable inductor in drawing 8 .
[Drawing 11] It is the circuit diagram showing the example of the anode plate pulse generating circuit in drawing 8 .
[Drawing 12] It is the circuit diagram showing the example of a configuration of the delay circuit in drawing 6 and drawing 11 .
[Drawing 13] It is the block diagram showing another example of the principle of operation.
[Drawing 14] It is the block diagram showing another example of the principle of operation.
[Drawing 15] It is drawing showing the pixel arrangement of a memory type PDP10 which is consulted when you understand the example of this invention.
[Drawing 16] It is the block diagram showing another example of the principle of operation.
[Description of Notations]
1 -- A video signal input terminal, 2 -- A synchronousr-control circuit, 3 -- A/D conversion and a memory circuit, 4 -- An auxiliary anode pulse generating circuit, 5 -- An anode plate pulse generating circuit, 6 -- Cathode pulse generating circuit, 7 -- An auxiliary anode driver, 8 -- A cathode driver, 9, 11, 12, 14, 31 -- Switch, 10 [-- NOR circuit,] -- A memory type PDP, 15 -- A capacitor, 13 -- An inductor, 42 52 -- A delay circuit, 53 -- An encoder, and S1 - Sm -- An auxiliary anode drive electrode and A1 -An -- An anode plate drive electrode and K1 -Kn -- [-- Cathode stray capacity] A cathode drive electrode, CS1 - CSm auxiliary anode stray capacity, CA1-CAn -- Anode plate stray capacity, Ck1-Ckn

[Translation done.]